AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A multi-ported orthogonal data memory for effecting a corner-turning function, where for example data input as a sequence of bit-parallel word-serial data transfers are converted to data output in a bit-serial, word-parallel fashion; the memory being arranged to transfer data words comprising a plurality of data items and comprising:

a plurality of data memory cells arranged in the form of a matrix having rows and columns, wherein the memory further comprises ~~and~~ a plurality of different and non-sequential groups of memory cells within the matrix, each group being:

i) a subgroup of the total number of memory cells in the matrix,

ii) having members of the group located in different rows and in different columns of the matrix, and

iii) being individually addressable to effect transfer of a data word thereto; and

enabling means having dedicated strobe connections to each of the plurality of groups of memory cells and being arranged to exclusively enable memory cells belonging to a selected ~~one~~s of the plurality of groups ~~of memory cells~~, as determined by the size of the data items being transferred, to read all of the data items of the data word present at their inputs into the selected group of memory cells or to write all of the data items of the data word stored in the selected group of memory cells to their outputs in a single transfer operation in a single clock cycle.

2. (Previously Presented) A memory according to Claim 1, wherein each of the groups of memory cells is specified according to its use in transferring the data items of the data word to or from the matrix to effect the corner-turning function.

3. (Previously Presented) A memory according to Claim 1, wherein the enabling means comprises selection means for selecting the current size of the data items in the data word and configuring the enabling means to operate with the selected current size of data items.

4. (Previously Presented) A memory according to Claim 3, wherein the number of different groups of memory cells provided within the matrix equals the number of different sizes of data items which can be handled by the memory.

5. (Previously Presented) A memory according to Claim 3, wherein each item of the data word being transferred is an integer power-of-two multiple of eight bits.

6. (Previously Presented) A memory according to Claim 1, wherein the memory is arranged to operate with different types of data words, each type comprising 64, 32, 16 or 8-bit data items.

7. (Canceled).

8. (Previously Presented) A memory according to Claim 1, wherein the enabling means is arranged to enable a selected group upon a set of logic conditions becoming true, the logic conditions being determined from a current selected row of the matrix and the size of the items being transferred.

9. (Previously Presented) A memory according to Claim 1, wherein the enabling means comprises a pointer in a shift register for determining which rows of the matrix are to be enabled for taking part in the data transfer of all of the data items of the data word.

10. (Previously Presented) A memory according to Claim 9, wherein the pointer in the shift register is configured to be operable in a plurality of different modes, each mode corresponding to a possible size of the data item being transferred, the pointer being configured within a single instruction to advance by a predetermined number of bit positions as determined by the current mode thereby indicating which rows of the matrix are to be enabled to facilitate transfer of the whole of the data word to or from the matrix.

11. (Previously Presented) A memory according to Claim 9, further comprising means for storing information relating to a faulty row in the matrix and wherein the shifting word pointer register is arranged to be controlled to skip the faulty row in the matrix and instead point to otherwise redundant additional row of the matrix.

12. (Previously Presented) A memory according to Claim 9, further comprising means for converting the current position of the row pointer in the shift register to one or more row select logic signals.

13. (Previously Presented) A memory according to Claim 12, further comprising a hard-wired backward propagation network for determining, from the bit position of the pointer and the size of the current data items, the rows of the matrix that are to be enabled for the data transfer.

14. (Previously Presented) A memory according to Claim l, wherein the enabling means comprises byte column determining means for enabling a specific group of byte column locations of the matrix within a selected word row to be enabled for transferring an item of the data word across a word port of the memory.

15. (Previously Presented) A memory according to Claim 14, wherein the byte column determining means comprises a table specifying the relationship between the plurality of different groups of memory cells and their respective memory cell locations in the matrix.

16. (Previously Presented) A memory according to Claim 1, wherein the enabling means comprises bit column determining means for enabling a specific group of bit column locations of the matrix within a selected word row to be enabled for transferring a bit of an item of the data word across a bit port of the memory.

17. (Previously Presented) A memory according to Claim 16, wherein the bit column determining means comprises a table specifying the relationship between the plurality of different groups of memory cells and their respective memory cell locations in the matrix.

18. (Previously Presented) A memory according to Claim 1, wherein the locations of the memory cells of each group form a repeating pattern when viewed as a matrix.

19. (Previously Presented) A memory according to Claim 1, further comprising a load register arranged to retain temporarily bit-serial word parallel data transferred to and from the matrix of memory cells across a bit port of the memory.

20. (Previously Presented) A memory according to Claim 1, further comprising a first masking register arranged to mask bits of the data to be read out of the matrix of memory cells via a bit port of the memory.

21. (Previously Presented) A memory according to Claim 1, further comprising a second masking register arranged to mask bits of the data to be input to the matrix of memory cells via a bit port of the memory.

22. (Currently Amended) A multi-ported orthogonal data memory for effecting a data corner-turning function between a plurality of SIMD associative processors and location addressable data store, the memory being arranged to transfer input data words comprising a plurality of data items across a word port for the data store and transfer data bits comprising an output word across a bit port for the SIMD associative processors, the memory comprising:

a plurality of data memory cells arranged in the form of a matrix having rows and columns, wherein the memory further comprises~~and~~ a plurality of different and non-sequential groups of memory cells within the matrix, wherein each group:

i) is a subgroup of the total number of memory cells in the matrix,

ii) has members of the group located in different rows and in different columns of the matrix,

iii) relates to a different size of data item, and

iv) is individually addressable to effect transfer of a data word thereto; and

enabling means having dedicated strobe connections to each of the plurality of groups of memory cells and being arranged to exclusively enable memory cells belonging to a selected one~~s~~ of the plurality of groups ~~of memory cells~~, as determined by the size of the data items being transferred, to transfer all of the data items of the input data word via the word port into the

selected group or bit data representing an output data word stored in the selected group via the bit port in a single transfer operation in a single clock cycle.

23. (Previously Presented) A memory according to claim 1 further comprising a plurality of SIMD associative processors.

24. (Previously Presented) A memory according to Claim 2, wherein the enabling means comprises selection means for selecting the current size of the data items in the data word and configuring the enabling means to operate with the selected current size of data items.

25. (Previously Presented) A memory according to Claim 3, wherein the enabling means comprises a pointer in a shift register for determining which rows of the matrix are to be enabled for taking part in the data transfer of all of the data items of the data word.